Remarks

Applicant respectfully requests reconsideration of this application. Claims 104-106, 110-112, 116-118 and 122-124 have been amended to correct minor informalities. No claims have been allowed.

Non-Art Rejections - 35 U.S.C. § 112

Claims 107, 108, 113, 114, 119, 120, 125 and 126 stand rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Specifically, the examiner considers that support is not found in the original disclosure for a first conduction channel with a thickness of 0.5 to 1.0 microns and the buried layer thickness of 1.0 to 1.5 microns.

Figure 12 and the corresponding discussion on page 23, line 6 through page 24, line 4, of the specification clearly shows a buried layer region formed at a distance between about 1.0 and 2.0 microns below the substrate surface. For example, the plot of Figure 12 shows an upper JFET conduction channel and a buried layer region both having a thickness of about 1.0 um. The specification on page 24, lines 2-3 explicitly states that the buried region is only about 1.0 um wide. The discussion on page 24, lines 5-11 further indicates that the buried region may be formed between about 0.5 to 2.0 um (i.e., 1.5 um thick). Figure 13 shows another embodiment with an upper JFET conduction channel of about 0.5 um thick. Hence, it is respectfully submitted that Applicant's disclosure supports the claimed range of thicknesses.

Claims 104-106, 110-112, 116-118 and 122-124 also stand rejected under 35 U.S.C. § 112, second paragraph, as being considered indefinite with respect to the term "charge" recited in the claims. Applicant has amended these claims to more distinctly claim the subject matter of the claimed invention by replacing "charge" with

the term -- doped impurity --. Accordingly, it is respectfully submitted that all claims now fully satisfy the requirements of the statute.

Art Rejections - 35 U.S.C. § 103(a)

Claims 1-4, 6-8, 10, 12-14, 17-19, 23, 58-78, 80-83 and 103-126 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Williams et al. (US 5,386,136; "Williams") in view of Yamanishi, et al. (JP404107877A; "Yamanishi"), or alternatively, obvious over Yamanishi in view of Williams. Additionally, claims 127 and 128 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Rumennik et al. (US 5,258,636; "Rumennik") in view of Yamanishi. Applicant respectfully submits that a *prima facie* case of obviousness does not exist with respect to the rejection of claims 1-4, 6-8, 10, 12-14, 17-19, 23, 58-78, 80-83 and 103-126, nor with respect to claims 127 and 128.

The office action asserts on page 8 that the existence of first and second conduction channels is inherent in Yamanishi's device structure. But a retrospective view of inherency is not a substitute for some teaching or suggestion which supports the selection and use of the various elements in the particular claimed combination. An allegedly inherent characteristic must *necessarily* flow from the teachings of the applied prior art. In this case, there is no teaching in Yamanishi that reasonably supports the conclusion that his device structure necessarily includes first and second conduction channels, with the meaning that those terms have in Applicant's claimed invention.

Applicant has submitted evidence traversing the obviousness rejection. This evidence, which supported a finding that a person of ordinary skill in the semiconductor arts in 1996 would not have had a reasonable expectation of success in combining the references in the manner proposed by the examiner, must be considered, but was not even addressed in the present Office Action. The

evidence further established that Williams' teaching of forming an extended drift region with a depth less than one micron would have discouraged one of ordinary skill in the art to make a modification or combination with Yamanishi to arrive at the claimed invention. The reason why is because an ordinary practitioner attempting to combine Williams with Yamanishi would have understood that a one micron deep N-type drift region is too shallow to permit formation of a buried region therein using Yamanishi's method of segregation of dopants by heat treatment. A person of ordinary skill in the art would therefore have lacked motivation to combine or modify Williams in view of Yamanishi to produce a device structure that includes dual JFET-type conduction channels above and below the buried region since there would have been no reasonable expectation that such an approach would work.

Applicant has also submitted evidence that any attempt by an ordinary practitioner to incorporate the feature of a p-type buried region according to Yamanishi into the shallow drift region 522 of Williams would have resulted in an inoperable device. Again, this evidence must be considered, but there is nothing in the Office Action to indicate that the examiner gave it proper consideration.

To establish a *prima facie* case of obviousness a rejection must show that there would have been a reasonable expectation of success by the hypothetical person of ordinary skill that the combination would work to produce beneficial results. In this case, the evidence shows that the person of ordinary skill would have lacked motivation to combine the references in the manner suggested by the Office Action because there was no reasonable expectation of success. There is nothing in the prior art to contradict this evidence.

It is the burden of the Examiner to set forth a *prima facie* case of obviousness. To carry this burden, the Examiner must establish why one having ordinary skill in the art would have been led to the claimed invention by the express teachings or suggestions found in the prior art, or by implications contained in such